REMARKS

Claim 1, for example, calls for delivering a first data from a first position in a first serial buffer having a receiving end to receive the first data and a delivering end opposite the receiving end. Second data is delivered from a second position in a second serial buffer. The second serial buffer has a receiving end to receive the second data and a delivering end opposite the receiving end. The first position relative to the delivering end of the first serial buffer is different than the second position relative to the delivering end of the second serial buffer.

Thus, referring, for example, to Figure 1 of the present application, a series of serial buffers 120a-120d are depicted. Each buffer includes a receiving end element 150a and a delivering end element 150h on the right side. The controller 140 determines if the data is to be delivered from a particular element 150 of each buffer 120. Thus, by delivering the data out from a selected element 150, deskewing can be achieved.

In contrast, in the cited reference to Vila, a series of buffers are utilized with test data therein. Each of the buffers are aligned using the test data. Thus, the data is always passed out through the same position, when the test sequence symbol T0, shown at T=n+1 in Figure 11, is received, the read pointer R is set. As subsequent symbols are received after the test sequence symbol, the write pointer is advanced so that each received data symbol will be stored in the buffer.

Thus, at times T=n+2 and T=n+3, data symbols 0 and 4 are received and stored in the buffer. Referring to Figure 12, this corresponds to the situation when all of the lanes are deskewed because the slowest, most retarded lane, lane 1, has now put the first bit of data into the buffer after having discovered its test sequence symbol T1. From thereon, all of the buffers have been deskewed. Then, as shown in Figure 13, the buffers are filled up with each of the lanes. However, it is clear that once each of the lanes are placed in the respective four buffers, those buffers will be read out from the same buffer positions for each lane.

Referring to Figure 13, the read pointer is pointed at the leftmost section of each buffer associated with each lane. Plainly, the reading occurs always from the first position to the left of each buffer. Therefore, the reference fails to meet the claimed limitations.

Particularly, the claim calls for delivering the data from a different position in different buffers in order to deskew. In the cited reference, the opposite is done. In the cited reference, the

data is always delivered from the same position of each buffer, that position being the leftmost position where the read pointer is always situated.

Therefore, claim 1 and its dependent claims should be in condition for allowance.

On a similar analysis, claim 7 and its dependent claims should be in condition for allowance. Also, claim 13 and its dependent claims should be in condition for allowance. For the same reasons, claim 21 and its dependent claims should be in condition for allowance.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation